Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please withdraw claims 2, 5-10, 12, 15-20, 22, 25-30, 34 and 37-42.

Listing of Claims:

1. (Original) A memory module, comprising:

a plurality of memory devices; and

a memory hub coupled to the memory devices, the memory hub comprising:

a link interface receiving memory requests for access to memory cells in at least one of the memory devices, at least some of the memory requests including respective memory hints providing information about the subsequent operation of the memory devices;

a memory device interface coupled to the memory devices and to the link interface, the memory device interface being operable to couple memory requests to the memory devices for access to memory cells in at least one of the memory devices and to receive read data responsive to at least some of the memory requests; and

a memory sequencer coupled to the link interface and the memory device interface, the memory sequencer being operable to couple memory requests to the memory device interface responsive to memory requests received from the link interface, the memory sequencer further being operable to dynamically adjust operability of the memory devices responsive to the memory hints.

2. (Withdraw) The memory module of claim 1 wherein the link interface comprises an optical input/output port.

3. (Original) The memory module of claim 1 wherein at least one of the hints comprises signals placing the memory devices in a page mode.

4. (Original) The memory module of claim 3 wherein at least one of the hints comprises a number of pages to remain open.

5. (Withdraw) The memory module of claim 1 wherein at least one of the hints comprises a prefetching hint.

6. (Withdraw) The memory module of claim 1 wherein at least one of the hints comprises a number of cache lines that will be sent.

7. (Withdraw) The memory module of claim 1 wherein at least one of the hints comprises a stride indicative of a sequence of addresses from which data are to be fetched.

8. (Withdraw) The memory module of claim 1 wherein at least one of the hints comprises a number of cache lines to skip.

9. (Withdraw) The memory module of claim 1 wherein the memory devices comprise dynamic random access memory devices.

10. (Withdraw) The memory module of claim 1, further comprising a request decoder coupled to the link interface and the memory sequencer, the request decoder being operable to decode the hint in the memory requests.

11. (Original) A memory hub, comprising:

a link interface receiving memory requests for access to memory cells in at least one of the memory devices, at least some of the memory requests including respective memory hints providing information about the subsequent operation of the memory devices;

a memory device interface coupled to the memory devices, the memory device interface being operable to couple memory requests to the memory devices for access to memory cells in at least one of the memory devices and to receive read data responsive to at least some of the memory requests; and

a memory sequencer coupled to the link interface and the memory device interface, the memory sequencer being operable to couple memory requests to the

memory device interface responsive to memory requests received from the link interface, the memory sequencer further being operable to dynamically adjust operability of the memory devices responsive to the memory hints.

12. (Withdraw) The memory hub of claim 11 wherein the link interface comprises an optical input/output port.

13. (Original) The memory hub of claim 11 wherein at least one of the hints comprises signals placing the memory devices in a page mode.

14. (Original) The memory hub of claim 13 wherein at least one of the hints comprises a number of pages to remain open.

15. (Withdraw) The memory hub of claim 11 wherein at least one of the hints comprises a prefetching hint.

16. (Withdraw) The memory hub of claim 11 wherein at least one of the hints comprises a number of cache lines that will be sent.

17. (Withdraw) The memory hub of claim 11 wherein at least one of the hints comprises a stride indicative of a sequence of addresses from which data are to be fetched.

18. (Withdraw) The memory hub of claim 11 wherein at least one of the hints comprises a number of cache lines to skip.

19. (Withdraw) The memory hub of claim 11 wherein the memory devices comprise dynamic random access memory devices.

20. (Withdraw) The memory hub of claim 12 further comprising a request decoder coupled to the link interface and the memory sequencer, the request decoder being operable to decode the hint.

21. (Original) A computer system, comprising:

a central processing unit ("CPU");

a system controller coupled to the CPU, the system controller having an input port and an output port;

an input device coupled to the CPU through the system controller;

an output device coupled to the CPU through the system controller;

a storage device coupled to the CPU through the system controller;

a plurality of memory modules, each of the memory modules comprising:

a plurality of memory devices; and

a memory hub coupled to the system controller and the memory devices, the memory hub comprising:

a link interface receiving memory requests from the system controller for access to memory cells in at least one of the memory devices, at least some of the memory requests including respective memory hints providing information about the subsequent operation of the memory devices;

a memory device interface coupled to the memory devices and to the link interface, the memory device interface being operable to couple memory requests to the memory devices for access to memory cells in at least one of the memory devices and to receive read data responsive to at least some of the memory requests; and

a memory sequencer coupled to the link interface and the memory device interface, the memory sequencer being operable to couple memory requests to the memory device interface responsive to memory requests received from the link interface, the memory sequencer further being operable to dynamically adjust operability of the memory devices responsive to the memory hint.

22. (Withdraw) The memory system of claim 21 wherein the link interface comprises an optical input/output port.

23. (Original) The memory system of claim 21 wherein at least one of the hints generated by the system controller comprises signals placing the memory devices in a page mode.

24. (Original) The memory system of claim 21 wherein at least one of the hints generated by the system controller comprises a number of pages to remain open.

25. (Withdraw) The memory system of claim 21 wherein at least one of the hints generated by the system controller comprises a prefetching hint.

26. (Withdraw) The memory system of claim 21 wherein at least one of the hints comprises a number of cache lines that will be sent from the system controller.

27. (Withdraw) The memory system of claim 21 wherein at least one of the hints generated by the system controller comprises a stride indicative of a sequence of addresses from which data are to be fetched.

28. (Withdraw) The memory system of claim 21 wherein at least one of the hints comprises a number of cache lines to skip.

29. (Withdraw) The memory system of claim 21 wherein the memory devices comprise dynamic random access memory devices.

30. (Withdraw) The memory system of claim 21, further comprising a request decoder coupled to the link interface and the memory sequencer, the request decoder being operable to decode the hint.

31. (Original) A method of adjusting memory sequencing in a memory module containing a plurality of memory devices, comprising:

generating memory requests for access to a memory device mounted on the memory module , at least some of the memory request including a memory hint; providing information about the subsequent operation of the memory devices;

receiving the memory requests at the memory module;

adjusting operability of memory module based on the memory hint; and

coupling the memory request to the memory device responsive to the received memory request.

32. (Original) The method of claim 31 wherein the act of adjusting operability of the memory module based on the memory hint comprises adjusting operability of the memory sequencer based on the memory hint.

33. (Original) The method of claim 31 wherein the act of adjusting operability of the memory module based on the memory hint comprises adjusting operability of the memory devices based on the memory hint.

34. (Withdraw) The method of claim 31 wherein the act of coupling the memory request to the memory device comprises coupling the memory request over a link interface comprising an optical input/output port.

35. (Original) The method of claim 31 wherein the act of adjusting operability of the memory module comprises placing the memory devices in page mode.

36. (Original) The method of claim 31 wherein act of adjusting operability of the memory module comprises leaving a number of pages open.

37. (Withdraw) The method of claim 31 wherein the hint generated by the system controller comprises a prefetching hint.

38. (Withdraw) The method of claim 31 wherein the hint generated by the system controller comprises a number of cache lines that will be sent.

39. (Withdraw) The method of claim 31, wherein the hint generated by the system controller comprises a stride indicative of a sequence of addresses from which data are to be fetched.

40. (Withdraw) The method of claim 31 wherein the hint comprises a number of cache lines to skip.

41. (Withdraw) The method of claim 31 wherein the memory devices comprise dynamic random access memory devices.

42. (Withdraw) The method of claim 31 further comprising decoding the hint with a request decoder.